

## ML12038 1.1 GHz Low Power Dual Modulus Prescaler

**Legacy Device:** Motorola MC12038A

The ML12038 can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Lansdale's ML145xxx series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 127/128 or 255/256 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- Low Power 4.8 mA Typical
- Operating Temperature Range  $T_A = -40^\circ$  to  $+85^\circ$ C
- Short Set Up Time (t<sub>set</sub>) 16ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible With Standard CMOS and TTL
- On-Chip Output Termination

## **FUNCTIONAL TABLE**

sw	МС	Divide Ratio
Н	Н	127
Н	L	128
L	Н	255
L	L	256

NOTES: 1. SW:  $H = V_{CC}$ , L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption. 2. MC: H = 2.0 V to  $V_{CC}$ , L = Gnd to 0.8 V.

Design Criteria	Value	Unit	
Internal Gate Count *	67	ea	
Internal Gate Propagation Delay	200	ps	
Internal Gate Power Dissipation	0.75	mW	
Speed Power Product	0.15	рЈ	

NOTE: \*Equivalent to a two-input NAND gate.

## **MAXIMUM RATINGS**

Characteristic	Symbol	Range	Unit			
Power Supply Voltage, Pin 2	VCC	-0.5 to 7.0	Vdc			
Operating Temperature Range	TA	-40 to 85	°C			
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C			
Modulus Control Input, Pin 6	МС	-0.5 to 6.5	Vdc			

P DIP 8 = PP PLASTIC PACKAGE CASE 626–04



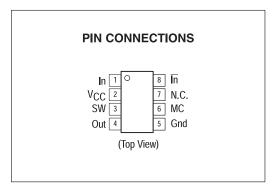


SO 8 = -5P PLASTIC PACKAGE CASE 751 (SO-8)

## **CROSS REFERENCE/ORDERING INFORMATION**

PACKAGE	<b>MOTOROLA</b>	LANSDALE
P-DIP 8	ML12038AP	ML12038PP
SO 8	ML12038AD	ML12038-5P

**Note**: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.



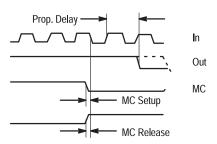
**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5 \text{ to } 5.5 \text{ Vdc}$ ,  $T_A = -40 \text{ to } 85^{\circ}\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.1	1.4	1.1	GHz
Supply Current Output Unloaded (Pin 2) at 5.0 Vdc	Icc	_	4.8	6.5	mA
Modulus Control Input High (MC)	V <sub>IH1</sub>	2.0	-	VCC	V
Modulus Control Input Low (MC)	V <sub>IL1</sub>	-	-	0.8	V
Divide Ratio Control Input High (SW)	V <sub>IH2</sub>	VCC	VCC	VCC	Vdc
Divide Ratio Control Input Low (SW)	V <sub>IL2</sub>	Open	Open	Open	_
Output Voltage Swing (C <sub>L</sub> = 8.0 pF)	V <sub>out</sub>	1.0	1.6	_	V <sub>pp</sub>
Modulus Setup Time MC to Out	<sup>t</sup> SET	_	11	16	ns
Input Voltage Sensitivity 250 to 1100 MHz 100–250 MHz	V <sub>in</sub> (min)	100 400	_	1500 1500	mVpp

Figure 1. Logic Diagram (ML12038)

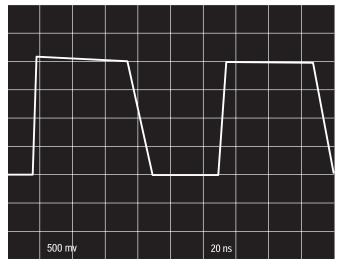
D D Q D Q С В C M QB C QB С QB MC Qв QB 4<sub>D</sub> D D QB D E G Н ○ Out ГС С QB С Q QB Q CSQ SW

Figure 2. Modulus Setup Time



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

Figure 3. Typical Output Waveform



 $(\div 128, 1.1 \text{ Ghz Input Frequency, V}_{CC} = 5.0 \text{ V}, TA = 25^{\circ}\text{C output Loaded})$ 

Figure 4. AC Test Circuit

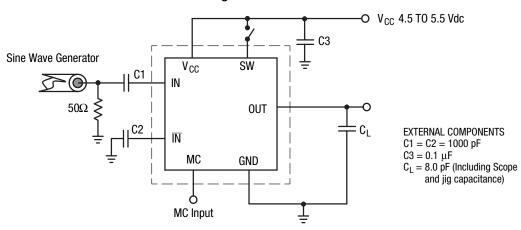
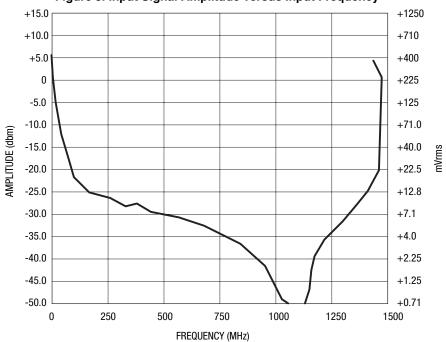
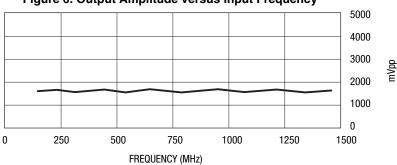


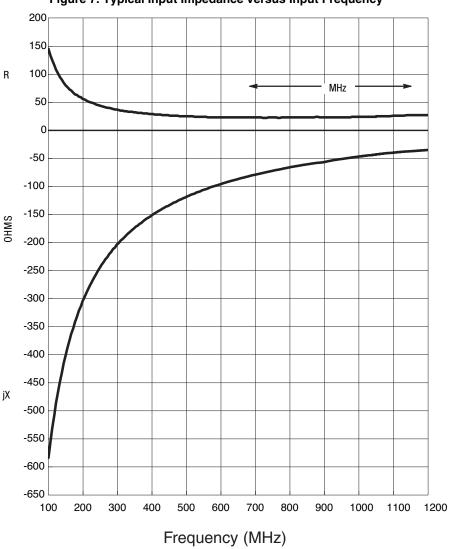
Figure 5. Input Signal Amplitude versus Input Frequency

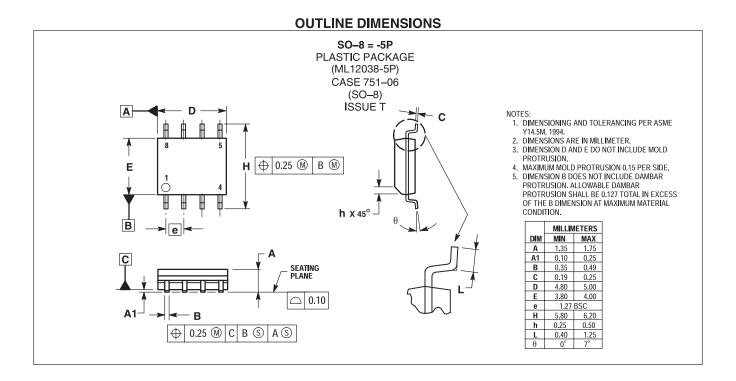


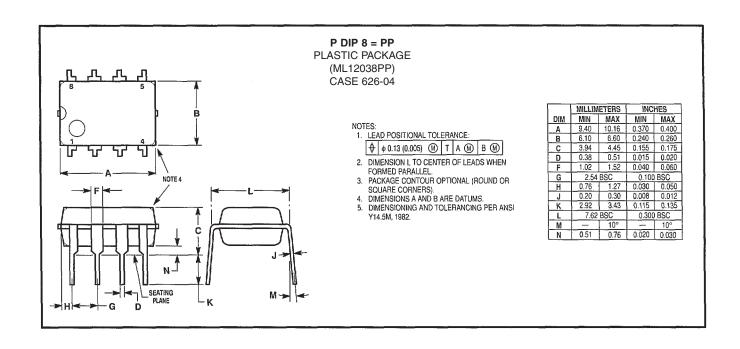
Divide Ratio = 128;  $V_{CC}$  = 5.0 V;  $T_A$  = 25°C

Figure 6. Output Amplitude versus Input Frequency









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